

CS 3443
Computer Systems
(traditional face to face)
Fall, 2020
Course Syllabus

Meeting Time and Place: MW 2:30 pm - 3:45 am, CLB 121

Required Textbook: *Computer Organization & Design, the Hardware/Software Interface*, Fifth Edition, Patterson and Hennessy

Instructor: N. Park

E-mail: npark(at)cs.okstate.edu

Course page: Canvas

Office: MSCS 211 (office)

Office Phone: 405-744-7937

Office Hours: MW 1:00-2:00pm (virtual)

Teaching Assistant: Asbhilah Kancharla (details to be posted on Canvas)

Prerequisite: CS 2113 (Computer Science I) and some basic C/Unix knowledge as needed

Tentative Grading:

- Programming/Homework Assignments and Quiz: 50%
- Exams (3, tentative): 10% each (Tentative Dates: Sep. 9, Oct. 7, Nov. 4)
- Final Exam (Comprehensive): 20% (Date: university schedule)

Tentative Grading Scale: [90-100%] A, [80-89%] B, [70-79%] C, [60-69%] D, [0-59%] F

Course Objective and Description: The objective of this course is to learn fundamental functional and register level description of computer systems, computer structures, addressing techniques, macros, linkage, input-output operations. Introduction to file processing operations and auxiliary storage devices. Programming assignments are implemented in assembly language.

Note: Homeworks and program assignments are due at the beginning of class on the date they are due (unless announced in class otherwise). Late homeworks will **not** be accepted. Late program penalty is **10%** per calendar day, according to the date and time on the printout. Only when verifiable extenuating circumstances can be demonstrated will

make-up exams or extended assignment due dates be considered. Verifiable extenuating circumstances must be reasons beyond control of the students, such as illness or accidental injury. Poor performance in class is not an extenuating circumstance. Advise your instructor of the verifiable extenuating circumstances in advance or as soon as possible. In such situations, the date and nature of the make-up exams and the extended due dates for the assignments will be decided by the instructor.

Attendance Policy: As this is an online course, regularly check your D2L page for the course.

Collaboration Policy: Discussion of techniques and ideas covered in class is encouraged. However, every line of on all assignments must be **your own**.

- In **programming assignments**, discussion of techniques in a natural language (such as English) is allowed, but a discussion in a computer or algorithmic language is not allowed. (Computer language discussions and questions are to be limited to the language and should not concern the assignment.) Stealing, giving or receiving any code, drawings, diagrams, texts or designs is not allowed.
- As for **examinations**, instructions will be provided how to arrange test center if needed one and etc beofre the exams.
- Students who do not comply with the above described collaboration policy will receive a grade of F in the course. Furthermore, the case will be reported to the University Officials.
- **50% Rule:** For any student to be eligible to receive a passing grade, the student must have earned at least 50% of the total points in each of two areas: (1) programs and other assignments, and (2) tests. Any student whose grades do not satisfy the 50% Rule will automatically receive a grade of F in the course regardless of the total points earned.

Course Outline:

1. Overview
2. Data Representation
 - Binary numbers
 - Conversion to/from binary, octal, hexadecimal
 - Floating point representation
3. Memory and Bit Operations
 - Lineary array of bytes

- Pointer
 - Bitwise operation
4. Instruction Set Architecture (ISA)
- Bridge between software and the processor (CPU)
 - Accumulator
 - Stack
 - General purpose registers
 - Load/store
5. MIPS ISA
- Assembler
 - Pseudo instructions
 - System calls
 - Procedure calls
 - SPIM, other ISAs
6. Basics of Logic Design
- Boolean functions
 - Logic gates
 - Multiplexers
 - Adder
 - Arithmetic logic unit (ALU)
7. The ALU and Memory Elements
- Circuit realization of a given boolean function
 - Add/subtract/overflow/compare/bitwise operation
 - Shifter
 - Memory elements: SR latch, D latch, D flip flop
 - Tri-state drivers and bus communication
 - Register files
 - Control signals
8. Integer and FP Arithmetic
- Integer multiplication

- Integer division
- Floating point arithmetic

9. Designing a Processor: datapath and control

- Single cycle datapath
- Single cycle control
- Multicycle datapath implementation
- Pipeline processor

10. Memory systems

- DRAM (dynamic random access memory)
- SRAM (static random access memory)
- Cache
- Virtual memory

11. InputOutput

12. Multiprocessor

Attachments: OSU Syllabus Attachment, Fall 2020 on Canvas